CE-ATA Technical Errata

Errata ID	**Protocol 008**
Affected Spec Ver.	**Protocol 1.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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Description of the specification technical flaw (add space as needed)

The DD_Cmd60W_RegWr state was allowed to be a blocking state as originally written in the CE-ATA 1.0 protocol specification. At this point in the protocol, the host believes that the corresponding MMC command is complete and that the next MMC command (CMD61) may be issued. Thus, it is inappropriate for DD_Cmd60W_RegWr to be a blocking state. This erratum makes that state non-blocking.

Description of the correction

The DD_Cmd60W_RegWr state in section 2.4.2.2.2 shall be modified as shown:

DD7: DD_Cmd60W_RegWr	Write received contents to MMC register addresses specified and notify ATA layer of register range that was updated.		
	1. Unconditional ~~Contents written and ATA layer notified~~	→	DD_Idle
	~~2. Contents not written or ATA layer not notified~~	→	~~DD_Cmd60W_RegWr~~

Disposition log

06/13/2005	Erratum captured
08/31/2005	Erratum ratified